

Appl. No. 09/555,301
Amendment and/or Response
Reply to Office action of 3 June 2004

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REMARKS / DISCUSSION OF ISSUES

Claims 4-20 are pending in the application. Claims 1-4 are canceled, and claims 5-20 are newly added.

The Examiner is respectfully requested to state whether the drawings are acceptable.

In the interest of advancing the prosecution in this case, the following remarks are provided with regard to Reiner (USP 5,995,629), which was the basis for rejection of claims 1-4 in the final Office action of 3 June 2004.

In claim 5, upon which claims 6-9 depend, the applicant claims a method of performing arithmetic operations and data transfers, wherein the arithmetic operations are performed substantially continuously, and dummy operations are performed during gaps in functional operations, so as to mask the power consumption associated with the functional operations.

Reiner teaches extending the application of a clock signal to an encoder so that the required time to perform functional operations is masked. Reiner does not teach or suggest performing operations substantially continuously.

In claim 10, upon which claims 11-16 depend, the applicant claims an integrated circuit comprising a processor, two data registers, and a controller, wherein the processor executes functional operations in a first time sequence and the controller is configured to control the transfers of data at the registers in a second time sequence that is substantially uncorrelated with the first time sequence, so that a correlation of first currents associated with performing the functional operations and second currents associated with performing the data transfers cannot be determined.

Reiner teaches extending the application of a clock signal to an encoder so that the required time to perform functional operations is masked; however, a correlation exists in Reiner between data transfers and the functional operations, because the functional operations start soon after the input data is received, and the output data is transferred after the (extended) operations are performed. Reiner does not teach the use of an additional buffer/register to isolate the times of data transfer from the times of processing.

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In claim 17, upon which claims 18-20 depend, the applicant claims an apparatus comprising a processor, two registers, and a controller, wherein the controller to control the transfer of a set of data between the second register and the first register corresponding to a sequence of functional operations performed by a processor, so that the transfer of the set of data between one of the registers and an other component is substantially uncorrelated to the sequence of functional operations performed by the processor.

Reiner teaches extending the application of a clock signal to an encoder so that the required time to perform functional operations is masked; however, a correlation exists in Reiner between data transfers and the functional operations, because the functional operations start soon after the input data is received, and the output data is transferred soon after the (extended) operations are performed. Reiner does not teach the use of an additional buffer/register to isolate the data transfers from the times of processing.

In view of the foregoing, the applicant respectfully requests that the Examiner withdraw the rejections of record, allow all the pending claims, and find the application to be in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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